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PATENT- OG VAREMÆRKESTYRELSEN

The present invention relates to a phase-locked loop comprising

a voltage controlled oscillator for generating an output signal and having a frequency control input for controlling the frequency of the output signal,

a divider for dividing the frequency of the output signal, and

a phase comparator for deriving a control signal from a phase error detected between the frequency-divided output signal and a reference signal, said control signal being coupled to the frequency control input of said voltage controlled oscillator

The invention also relates to a method for determining the phase error between a first signal and a second signal and a phase comparator for carrying out the method

Phase-locked loops of the above-mentioned type are used in a variety of applications In general, and as described above, phase-locked loops include a phase comparator or phase detector to compare the phase of a frequency-divided output signal of the voltage controlled oscillator and a reference signal The difference between these two signals is used to generate a control signal or error signal which is fed back to the voltage controlled oscillator so as to control the frequency of its signal output in a direction that reduces this phase difference For example, phase-locked loops are used in different types of radio systems, such as cellular phones, in which an oscillator is locked to an accurate reference frequency Different means are then provided to scale this accurate reference frequency to the desired frequency

In a conventional phase-locked loop (PLL) of the above-mentioned type it is well known to divide the output signal of the voltage controlled oscillator (VCO) by a natural number (N_0) As mentioned the division is performed by a divider or frequency divider The reason to perform the division is because comparators according to the prior art only are able to compare the phase of two signals if the frequency of the two

signals to be compared are equal and because the because the output frequency usually is "high" (MHz or GHz range) it is easier/more feasible to have the control circuit to work at a lower frequency In some embodiments the reference clock may also be divided by a natural number (N_R) by a frequency divider in order to obtain a given frequency of the two signals to be compared

When using a phase-locked loop of the above-mentioned type some unwanted frequency components or spurious occur in the output signal These spurious occur as a result of the phase comparator (also called phase detector) working at a frequency given hereby The spurious are an unwanted effect as it most often reduces the overall performance of the system in which the phase-lock loop is operating For example, spurious on the carrier in a radio system is a disadvantage as it causes undesired channels to interfere with the desired channel and thereby reducing the over-all performance of the radio system

According to the prior art, a solution to this problem is to filter out the spurious by use of a loop filter, most often located between the phase comparator and the voltage-controlled oscillator, i e the control signal for the voltage-controlled oscillator is filtered Generally the spurious can be filtered out in a loop filter if the bandwidth of the loop filter is significantly small, e g smaller than the distance between the spurious But the price of reducing the bandwidth of the loop filter is a slower PLL, i e the lock-in time for the PLL is increased

Some if not most prior art phase-locked loops, which are fully or partly implemented using digital components, also have a risk of producing sub-harmonic frequencies due to the way they are implemented This is due to the way the two signals, the reference signal and the output signal, interact with each other Ideally the reference signal and the output signal operates asynchronous, where the phase lock is established when the phases coincide Until this happens and if a disturbance breaks the lock there may occur sub-harmonics

US 5459435 shows a digital implementation of a PLL The invention is a straight forward conversion of the known analog PLL topology, where a first and a second counter unit is used to indicate the phase error between the frequency divided output signal and the reference The resolution of the PLL is fixed to the bit resolution of the digital implementation thus fixing the ratios between output frequency and reference frequency

US 5999060 also shows a digital implementation of a PLL using counters As with US 5459435 the resolution of the PLL is firstly fixed to the bit resolution, but is secondly compensated by a scaling means in the feed back The scaling means gives the possibility to increase the number of possible output frequencies

US 6188288 is similar in many ways to US 5999060 in that some scaling means is used in the feed back to compensate for the bit resolution US 6188288 differs from the above mentioned PLL's in that a current controlled oscillator is used and not a voltage controlled oscillator

The above mentioned PLL introduces means for increasing the number of possible output frequencies They also increase the complexity of the PLL-circuit considerably and do not improve on the lock-in time for the PLL, because a loop filter with a narrow bandwidth is still needed

The object of the invention is to provide an improved phase-locked loop compared to the phase-lock loop of the prior art, with a fast lock-in time, minimum risk for sub-harmonics in the output and a simple circuit

According to the invention, the object is achieved by a phase-locked loop of the above-mentioned type characterised in that said phase detector includes

a first accumulator adapted to add a first predefined phase step value to a first accumulated phase value in response to a reoccurring event in said frequency-divided output signal,

a second accumulator adapted to add a second predefined phase step value to a second accumulated phase value in response to a reoccurring event in said reference signal, and

subtracting means for determining the phase error by subtracting the second accumulated phase value from the first accumulated phase value

A PLL of this type has a large loop-bandwidth, which is independent of the division ratio and consequently a fast lock-in time The loop-bandwidth may be large because, as shown later, the spurious in the output may to a large degree may be placed as desired, thus allowing for a loop-filter with a wider bandwidth

Because the loop-bandwidth is larger, the time-constant of the loop is smaller Therefore it is cheaper to integrate because the sizes of the loop-components are smaller and thereby take up a smaller die array

Because the loop-bandwidth is independent of the division ratio, the PLL can compensate for frequency errors in references, and thereby eliminate the need of using voltage controlled temperature compensated crystal oscillators (VCTXCO) or voltage controlled crystal oscillators (VCXO), which is used in nearly all wireless radio systems and other radio systems VCTCXO and VCXO is normally an expensive circuit and can be replaced with a more simple crystal oscilator which normally has better phase noise performance than VCTCXO and VCXO

Also, because the loop-bandwidth is larger it is possible to suppress narrowband phase noise of the VCO in a wider bandwidth around the carrier and hereby improving the overall performance of the PLL This means that VCO does not have to have as good narrowband phase-noise performance as for a traditional PLL system Because resonators on an integrated circuit has very low Q-values, the performance of integrated VCO are usually not as good as a discreet solution In some systems this gives the possibility to fully integrate the VCO where it would not be possible using a traditional system

Further, because the PLL has a fast lock-in time, it is possible to direct-digital-modulate the PLL by changing N_R and and N_V values This means that the up-converter can be eliminated in systems using frequency shift keying (FSK) and phase shift keying (PSK)

According to a preferred embodiment of the invention, the phase comparator includes a digital-to-analogue converter adapted to convert the phase error and thereby to generate an analogue output signal Hereby the phase-locked loop achieves a very large internal amplification - amplification that approaches infinite - so the bandwidth of the phase-locked loop is determined primarily by the loop filter

According to a preferred embodiment of the invention, the phase comparator includes a first and a second digital-to-analogue converter adapted to convert the first and the second accumulated phase value and thereby to generate analogue representations thereof, and that the subtracting means are adapted to perform an analogue subtraction of the analogue representation of the second accumulated phase value from the analogue representation of the first accumulated phase value This is advantageous due the fact that the reference signal and the output signal essentially operate asynchronously Using an analogue subtraction, the forward look-up tables of the digital to analogue that otherwise may cause a ripple in the output, will reduce or eliminate these ripples

According to a preferred embodiment of the invention, the phase comparator includes a first and a second AND-means, where the output of said first AND-means is connected to a first digital-to-analogue converter, whereby a first accumulator is connected to a first non-inverting input of said first AND-means and whereby a second accumulator is connected to a first inverting input of said first AND-means, the output of said second AND-means being connected to said second digital-to-analogue converter, and that said second accumulator further is connected to a first non-inverting input of said second AND-means, said first accumulator further being connected to a first inverting input of said second AND-means The digital-to-analogue converters have a settling time - the time from a digital input is applied to the digital-to-analogue converter until a stable output is achieved - which may cause large but short lived errors when the more-significant bit changes, especially the most significant bit This is especially a problem, because the reference signal and the output signal essentially operate asynchronously Furthermore, due to the way digital addition (subtraction) is done inside the component, there may be a short ripple in the output from the component By using an AND-means, the digital number is pre-processed, facilitating a more error-free output from the digital-to-analogue converter

According to a preferred embodiment of the invention, the phase comparator includes a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator, and a third AND-means, where the output of said third AND-means is connected to said first and said second reset means of said first and said second accumulator, where the most significant bit of said first accumulator is connected to a first non-inverting input of said third AND-means, and where the most significant bit of said second accumulator is connected to a second non-inverting input of said third AND-means The intended output from the phase comparator is the phase difference between the two signals and not their absolute value By using reset means for the most significant bit of said first and second accumulator numerical overflows of the accumulators are prevented and at the same time the output from the phase comparator remains the same As described

above, the resets are of the most significant bits of the accumulator and controlled by the most significant bits of the input to the digital-to-analogue converter Exactly the same function may be achieved by using any of the bits and any number of resets

The invention also relates to a method of detecting the phase error between a first signal and a second signal, where the method includes the steps

frequency dividing the first signal and/or the second signal,

generating a first reoccurring trigger event in response to the first signal,

generating a second reoccurring trigger event in response to the second signal,

incrementing a first phase value by a first predetermined increment value when the first trigger event occurs,

incrementing a second phase value by a second predetermined increment value when the second trigger event occurs,

calculating said phase error by subtracting said second phase value from said first phase value

The invention also relates to a phase comparator (103) for carrying out the above mentioned method

The phase error calculated by the above method may be used to control a VCO like the one used with a PLL If the method is e g implemented in a digital signal processor (DSP), the voltage used to control the VCO may be generated by converting the digital number representing the phase error to a output voltage from the DSP The described method is, however, also useful whenever a phase error is needed between

two signals

Constructing a phase-locked loop as described above have a number of benefits These benefits may most easily be seen from an analysis of the circuits function Starting with analysing the above mentioned phase-locked loop in an ideal non-digital case, the phase versus time of the output signal and the reference signal may be represented as

$$\begin{aligned} \phi_R(t) &= \omega_R t + \phi_{R0} \\ \phi_V(t) &= \omega_V t + \phi_{V0} \end{aligned} \qquad [1]$$

where index R is the reference and index V is the variable frequency

The period time T_R and T_V of the signal may be calculated as

$$T_R = \frac{2\pi}{\omega_R} \text{ and } T_V = \frac{2\pi}{\omega_V} \qquad [2]$$

The fractional relationship between T_R and T_V as

$$\begin{aligned} T_R &= N_R \Delta t \quad , \quad \frac{1}{2} N_R \in \mathbb{N} \\ T_V &= N_V \Delta t \quad , \quad \frac{1}{2} N_V \in \mathbb{N} \end{aligned} \qquad [3]$$

where N_R and N_V are the integer numbers by which the frequencies are divided

From [1], [2] and [3] the following relation may be defined as

$$\begin{aligned} N_R \phi_r(t) &= \frac{2\pi}{N_R \Delta t} N_R t + N_R \phi_{R0} \\ N_V \phi_r(t) &= \frac{2\pi}{N_V \Delta t} N_V t + N_V \phi_{V0} \end{aligned} \qquad [4]$$

The phase error may be defined as

$$\epsilon(t) = N_R \phi_R(t) - N_V \phi_V(t) \qquad [5]$$

If the relations in [3] and [4] are fulfilled, the slope of the phase functions may be derived as $N_R \phi_R(t)$ and $N_V \phi_V(t)$, where both of the slopes are equal to $K_\phi = 2\pi / \Delta t$ This leads to the following error relation

$$\epsilon(t)\Big|_{\frac{\omega_R}{\omega_V}=\frac{N_V}{N_R}} = N_R\phi_{R0} - N_V\phi_{V0} \qquad [6]$$

This means that the phase error function is equal to the traditional PLL when $\frac{\omega_R}{\omega_V} = \frac{N_V}{N_R}$ When $N_R = N_V = 1$, the phase error is exactly the same as a traditional PLL Laplace transforming [4], the spectral domain becomes

$$\begin{aligned} P_R(s) &= \mathcal{L}\left\{\frac{N_R}{2\pi}\phi_R(t)\right\} = \frac{N_R\omega_R}{2\pi s^2} + \frac{N_R}{2\pi}\phi_R = \frac{N_R}{T_R s^2} + \frac{N_R}{2\pi}\phi_R \\ P_V(s) &= \mathcal{L}\left\{\frac{N_V}{2\pi}\phi_V(t)\right\} = \frac{N_V\omega_V}{2\pi s^2} + \frac{N_V}{2\pi}\phi_V = \frac{N_V}{T_V s^2} + \frac{N_V}{2\pi}\phi_V \end{aligned} \qquad [7]$$

In the ideal case, the phase function of the PLL is a straight line with a slope In the digital implementation of a PLL, the phase function becomes a staircase function This corresponds to an error function between the straight line and the staircase which is a sawtooth function From [4] the staircase phase function may be defined as

$$\begin{aligned} r(t)\Big|_{t=T_{Ri}} &= \frac{N_R}{2\pi}\phi_R(t)\Big|_{t=T_{Ri}}, \quad i \in \mathbb{N}^0 \\ v(t)\Big|_{t=T_{Vj}} &= \frac{N_V}{2\pi}\phi_V(t)\Big|_{t=T_{Vj}}, \quad j \in \mathbb{N}^0 \end{aligned} \qquad [8]$$

which in the continuous time domain gives the staircase phase function as

$$\begin{aligned} r(t)\Big|_{t\in\left]T_{Ri}-\frac{T_R}{2}\ T_R(i+1)\frac{T_R}{2}\right]} &= \left(\frac{N_R}{T_R}\Delta t\right)i + \frac{N_R}{2} + N_R\frac{\phi_{R0}}{2\pi} \\ v(t)\Big|_{t\in\left]T_{Vi}-\frac{T_V}{2}\ T_V(i+1)\frac{T_V}{2}\right]} &= \left(\frac{N_V}{T_V}\Delta t\right)i + \frac{N_V}{2} + N_V\frac{\phi_{V0}}{2\pi} \end{aligned} \qquad [9]$$

and which in the spectral domain may be written as

$$\mathcal{L}\{r(t)\} = R(s) = \frac{N_R}{s\left(1 - e^{-T_R s}\right)} e^{-T_R s} + N_R + N_R \frac{\phi_{R0}}{2\pi}$$
$$\mathcal{L}\{v(t)\} = V(s) = \frac{N_V}{s\left(1 - e^{-T_V s}\right)} e^{-T_V s} + N_V + N_V \frac{\phi_{V0}}{2\pi} \quad [10]$$

$$R(s) = \left\{\frac{N_R}{s\left(1 - e^{-T_R s}\right)} - \frac{N_R}{T_R s^2} - \frac{N_R}{2}\right\} + \frac{N_R}{T_R s^2} + \frac{N_R}{2\pi}\phi_{R0}$$
$$V(s) = \left\{\frac{N_V}{s\left(1 - e^{-T_V s}\right)} - \frac{N_V}{T_V s^2} - \frac{N_V}{2}\right\} + \frac{N_V}{T_V s^2} + \frac{N_V}{2\pi}\phi_{V0} \quad [11]$$

From [7] and [11] the following relation may be defined as

$$R(s) = S_R(s) + P_R(s)$$
$$V(s) = S_V(s) + P_V(s) \quad [12]$$

From [11] and [12] the time domain functions for s_R and s_V may be derives as

$$s_R(t)\Big|_{t \geq 0} = \mathcal{L}^{-1}\{S_R(s)\} = -\frac{N_R}{\pi}\sum_{k \in N^0}(-1)^k \frac{\sin((2k+1)\omega_R t)}{2k+1}$$
$$s_V(t)\Big|_{t \geq 0} = \mathcal{L}^{-1}\{S_V(s)\} = -\frac{N_V}{\pi}\sum_{k \in N^0}(-1)^k \frac{\sin((2k+1)\omega_V t)}{2k+1} \quad [13]$$

The phase error function from [5] may be derived in a similar manner as

$$e(t) = r(t) - v(t) = \epsilon(t) + s_R(t) + s_V(t) \quad [14]$$

where the only difference between the two functions is the sawtooth function given by [13], which in the spectral domain becomes

$$\mathcal{E}(s) = R(s) - V(s) \quad [15]$$

Analysing the staircase error function, it appears that there are no spectral harmonics below ω_R or ω_V This means that there are no sub-harmonics of the reference signal nor the variable signal

From the above the selected output frequency becomes a function of the reference frequency and the integers by which the frequencies are divided as

$$f_O = \frac{N_V}{N_R} N_F f_R \qquad [16]$$

According to [13] the generated spurious may be selected to be as far apart as desired by selecting the two integers N_R and N_V appropriately, because it is their ratio that selects the output frequency Also, according to [13], the amplitude of the spurious decreases the further away from the base frequency they are This provides a large loop-bandwidth, which means a fast lock-in time It is therefor both possible to select the bandwidth of the loop and how closely the spurious are placed, thereby producing a component which is more like the ideal phase-locked loop, without some of the disadvantages due to the way the component is constructed The phase-locked loop is also easily constructed with standard "of-the-shelf" components

Other features and advantages of the method of the present invention will become apparent from the following description of preferred embodiments, taken in conjunction with the accompanying figures wherein

Figure 1 is an example of a phase-locked loop according to the prior art,

Figure 2 is a first embodiment of a phase comparator or frequency comparator according to the invention,

Figure 3 is a second embodiment of a phase comparator or frequency comparator according to the invention,

Figure 4 is a third embodiment of a phase comparator or frequency comparator according to the invention, and

Figure 5 illustrates a phase-locked loop according to the invention

In the figures are all lines with a small line across representing a binary number Figure 1 is an example of a phase-locked loop according to the prior art The phase-locked loop 100 includes a voltage controlled oscillator 101, a frequency divider 102, and a phase comparator 103 The voltage controlled oscillator or VCO 101 includes a frequency controlling input terminal and an output terminal As shown in the figure, the output terminal of the VCO 101 is operatively connected to an input terminal of the frequency divider 102 Further, the frequency divider 102 includes an output terminal which is operatively connected to a first input terminal of the phase comparator 103 The phase comparator 103, which is also denoted a phase detector 103 in the following, also includes a second input terminal and an output terminal The output terminal of the phase detector 103 is operatively connected to the input terminal of the VCO 101 Hereby the voltage controlled oscillator 101, the frequency divider 102, and the phase comparator 103 form a closed loop

The voltage controlled oscillator or VCO 101 is adapted for retrieving an control signal via the input terminal of the VCO and for generating an oscillating electrical output signal having a frequency which is determined by the control signal The frequency divider 102 is adapted for dividing the frequency of a signal supplied thereto, i e the output signal of the VCO 101, and hereby generating a signal having a reduced frequency compared to the frequency of the input signal supplied thereto

The phase comparator 103 is adapted for deriving a control signal from the frequency-divided output signal and a reference signal supplied thereto via the first and the second input terminal, respectively Hereby, when the phase comparator 103 is supplied by the frequency-divided output signal from the VCO 101 and the reference signal, an output signal reflecting the phase error between the two input signals is generated For example, the phase comparator may output a voltage proportional to the phase difference between the input signals As mentioned above, the phase comparator 103 is coupled to the voltage controlled oscillator 101, i e during operation the control signal generated by the phase comparator 103 is supplied to the VCO 101 via the

frequency control input terminal of said voltage controlled oscillator

The shown phase-locked loop also includes a loop filter 105 adapted for smoothening the output of phase detector 103, i e filtering the signal used to control the voltage controlled oscillator 101 and hereby reducing unwanted spurius occurring in the signal Further, as illustrated in the figure, the frequency divider 102 may include one or more frequency dividing parts 102A, 102B Hereby, a first frequency dividing part 102A and a second frequency dividing part 102B may be adapted for performing the frequency division in two successive steps In addition, the reference signal may also be derived from another signal, e g the reference signal may be an output signal of a frequency divider 109 as shown in the figure

In short the operation of a phase-locked loop may be explained as follows During operation the frequency divider 102 receives an oscillating input signal from the VCO and generates an oscillating signal having a reduced frequency The phase detector 103 outputs a signal which is determined by the phase difference between the two input signals supplied thereto, ie the phase difference between the output signal of the frequency divider 102 and the reference signal When the phase of the output signal from the frequency divider 102 lags behind of the phase of the reference signal, the phase detector outputs an "up" signal, e g by increasing the output voltage which is supplied to the VCO 101 via the loop filter 105 On the other hand, when the phase of the output signal from the frequency divider 102 leads that of the reference signal, the phase detector outputs a "down" signal, e g by decreasing the output voltage which is supplied to the VCO 101 via the loop filter 105 The voltage controlled oscillator 101 outputs an oscillating signal determined by the output voltage from the loop filter 105 Hereby, the frequency of the VCO output signal increases and decreases when the phase detector 103 outputs an "up" and a "down" signal, respectively As a result the phase difference between output signal of the frequency divider 102 and the reference signal is decreased When the phase-locked loop 100 is in a phase-locked state, the phase of the output signal of the frequency divider 102 is in alignment with

that of the reference signal and the frequency of the two signals are the same There is therefor three signals of importance in the phase-locked loop A_0, A_V and A_R which are cyclic functions and may be described as

$$\begin{aligned} A_0(t) &= \sin(\omega_0 t + \phi_0) \\ A_R(t) &= \sin(\omega_R t + \phi_R) \\ A_V(t) &= \sin(\omega_V t + \phi_V) \end{aligned} \qquad [17]$$

When the system is in lock the following condition is fulfilled

$$\omega_D = \frac{\omega_R}{N_R} = \frac{\omega_V}{N_V} = \frac{\omega_0}{N_V \; N_F} \qquad [18]$$

which gives a phase error

$$\phi_D = \frac{\phi_R}{N_R} - \frac{\phi_V}{N_V} \qquad [19]$$

The effective frequency by which the phase comparator operates is that which corresponds to ω_D This will lead to the generation of spurious, because this frequency is slower than ω_0 The spurious are unwanted, because they will cause unwanted channels to interfere and must be filtered out by a filter placed in the loop However, this reduces the bandwidth of the phase-locked loop

Figure 2 illustrates a first embodiment of a phase comparator or frequency comparator according to the invention The phase comparator includes a first accumulator 201, a second accumulator 202 and subtracting means 203 The first accumulator 201 and the second accumulator 202 both include an input terminal and an output terminal The first and the second accumulator 201, 202 are operatively connected to a first and a second input terminal of the subtracting means 203 The first and the second accumulator 201, 202 are both adapted for receiving an input signal via the input terminal and generation an output signal which is supplied to the subtracting means Responsive to the input signal received via the input terminal of the accumulator 201, the first accumulator 201 is adapted for accumulating a first value in a register or memory thereof Likewise, responsive to the input signal received via the input terminal of the accumulator 202, the second accumulator 202 is adapted for

accumulating a second value in a register or memory thereof The phase comparator is adapted for supplying the first and the second accumulated values to the subtraction means 203 and thereby the difference there between may be determined When the first and the second accumulator 201, 202 are adapted for being triggered by trigger signals reflecting the phase of a first and a second signal, respectively, the difference between the accumulated values reflects the phase difference between the first and the second signal

In the shown embodiment, the first accumulator 201 includes a first digital register 208, a second digital register 209, a first adder 210 and a first trigger 205 The first adder 201 is adapted for being supplied with the contents of the two registers 208, 209 or at least a subset thereof, e g a number of the least significant bits, as input values The first adder 210 is adapted for adding the values supplied as input and hereby generating a digital output signal The output of the adder 210 is connected to the input of the first register 208 which is adapted for being trigged by a trigger signal supplied thereto via the first trigger 205 connected thereto When the first register 208 is trigged, the input value supplied thereto by the adder 210 written into the first register 208 and hereby saved as the new updated content thereof. For simplicity, in the shown embodiment the contents of the registers 208 and 209 are continuously present at the output terminals As a result the output of the first adder 210 is present at the input terminal of the register 208 and therefore the content is updated when the register 208 is trigged by trigger means 205

When the second register 209 holds a predefined phase step value, the first register 208 includes a first accumulated phase value which is updated when trigged A first oscillating signal $A_R(t)$, e g a reference signal, may be supplied as input to the first trigger means 205 and hereby the first trigger means 205 forms a trigger signal which is supplied to the first register 208 As indicated in Figure 2, the first trigger means 205 is adapted for trigging the first register 208 when a first input signal supplied thereto exceeds a first predetermined level, i e the first accumulator 201 is adapted

for, responsive to a reoccurring event in a first oscillating signal supplied thereto, adding a first predefined phase step value to a first accumulated phase value

In the shown embodiment, the second accumulator 202 is implemented similarly to the above-mentioned implementation of the first accumulator 201, and includes two registers 211, 212, a second adder 213, and a second trigger 206 The output of the second trigger 206 is connected to a trigger input of a first of the two registers A second oscillating signal $A_V(t)$, e g a frequency-divided version of an voltage controlled oscillator output signal, may be supplied as an input to the second trigger 206 As indicated, the second trigger 206 is adapted for trigging the first of the two registers 211 when a second input signal supplied thereto exceeds a second predetermined signal level, i e the second accumulator 202 is adapted for, responsive to a reoccurring event in the second oscillating signal supplied thereto, adding a second predefined phase step value to a second accumulated phase value When the first of the two registers is trigged the output of the second adder 213, i e the sum of the contents of the two registers 211, 212, is stored as the new content of the register 211

When a first and a second oscillating signal are supplied to the first and the second trigger means 205, 206, respectively, and when the second and the fourth registers 209, 212 are given a value representing a predefined phase step, the outputs of the first and the second accumulator are accumulated phase values reflecting the phase of the first and the second oscillating signal, respectively The subtracting means 203 is adapted for subtracting the first accumulated phase value and the second accumulated phase value and hereby determining the phase error between the first and the second signal supplied to the trigger means 205, 206 As illustrated in the figure, the output of the subtracting means 203 is connected to a digital-to-analogue converter 204 adapted for converting the digital representation of the phase error to an analogue value and hereby forming and analogue output signal of the phase comparator

The predefined phase steps could be selected from a maximum allowable phase accuracy, which with 16 bit resolution would be

$$\frac{360°}{2^n} = \frac{360°}{2^{16}} \approx 0\,005° \qquad [20]$$

It is however not required to select the predefined phase steps based on the bit resolution according to [16] many integer numbers may be selected giving the possibility of selecting placement of spurious as well as the frequency scaling between the reference signal and the output

The above-mentioned embodiment is advantageous due to the simplicity which is obtained due to the calculation of the phase error as a digital subtraction The price, on the other hand, is that the digital subtraction may generate spikes and hazards in the resulting phase error signal In the following a second embodiment of a phase comparator according to the invention is described This embodiment is an example of a phase comparator which is both simple and hereby easy to implement, and in which spikes and hazards do not occur in the resulting output signal

Figure 3 illustrates a second embodiment of a phase comparator according to the invention. In this embodiment, the first and the second accumulator 201, 202 is implemented as described in relation to figure 2 Therefore the first and the second accumulator 201, 202 and the function thereof will not be described further below

In contrast to the embodiment shown in figure 2, the output of the first and the second accumulators 201, 202 in the embodiment shown in figure 3 are connected to a first and a second digital-to-analogue converter 204A, 204B, respectively Hereby, when a digital value representing an accumulated phase value is supplied the first and the second digital-to-analogue converter 204A, 204B, respectively, an analogue representation thereof is formed The output of the first and second digital-to-analogue converter 204A, 204B are connected to a subtraction means 223 which is adapted for performing an analogue subtraction and hereby forming an analogue output signal of

the phase comparator

Optionally the phase comparator may include a first and a second AND-gate 220, 221 as illustrated in figure 3 In the shown embodiment, the output of the first accumulator 201 and the second accumulator 202 is connected to a non-inverted and an inverted input of the first AND-gate 220, respectively Further, the output of the first accumulator 201 and the second accumulator 202 is connected to an inverted and a non-inverted input of the first AND-gate 220, respectively As illustrated in the figure, the AND-gates 220, 221 are adapted for performing a bit-by-bit AND operation on the digital signals supplied thereto This may be explained in the following way When each of the bits are added or subtracted, the outcome from one set of bits affects the outcome from others As an example if 1 is added to the digital number 111 the result is 1000, which is straight forward However, what happens is a bit-by-bit approach, where 1+1=0 plus a 1 for the next bit As the AND-gate is not triggered, this will cause a rippling effect on the output Using AND-gates as described above, the subtraction of the two digital numbers is pre-processed By further digital-to-analog converting the digital numbers with the two digital-to-analogue converters 204A, 204B and performing the subtraction with as an analog subtraction means 223, the risk of ripples are significantly minimised

The analogue subtraction means in the above-mentioned phase comparator is advantageous as no spikes or hazards will occur in the resulting output signal due to short lived error signals on the higher bits Therefore, this embodiment has been found very useful

The two adding means 210 and 213 does not contribute to a similar problem as described above This is because the output from the two adding means 210 and 213 are only read into said first digital register 208 and said second digital register 209 when they are triggered by said first trigger 205 or said second trigger 206 The outputs from said two adding means 210 and 213 therefore have adequate time to settle

to stable outputs

Figure 4 illustrates a third embodiment of a phase comparator according to the invention The shown embodiment includes a synchronous reset of the most significant bit (MSB) of the first register 208 and the third register 211, i e the registers adapted for including accumulated values It is, however, not the absolute value of the digital number in the registers, but the difference between the numbers The synchronous reset may be implemented as illustrated in figure 4 In the shown embodiment the first register 208 and the third register 211 have the same length, i e the two registers include the same number of bits When the phase comparator is in use the contents of the two registers are accumulated as a result of the above-mentioned trigger signal supplied thereto As the difference between the contents of the two registers is calculated, it has to be insured that a possible overflow of the registers is taken care of This is due to the fact that an uncontrolled overflow may otherwise lead to an undesired result when performing the subsequent subtraction To overcome this problem an AND-gate 404 is connected to the first and the third register 208, 211 The AND-gate 404 is adapted for being supplied with the most significant bit (MSB) of the first register 208 and the third register 211 as shown in the figure The output of the AND-gate 404 is connected to a reset input of both the first register 208 and the third register 211 Hereby, when the most significant bit of both the first and the third register 208, 211 is "1" , i e the MSB equals a value of logical "1", the output value of the AND-gate 404 is also "1" In all other situations, the output value of the AND-gate 404 is "0" Therefore the most significant bit of the first and the third register is reset, i e set to "0", when they have both become "1" Hereby, an overflow is avoided in such a manner that the output signal of the phase comparator continuously reflects the phase difference between the two input signals supplied thereto Optionally, a similar reset may be implemented for not only MSB, but for any bit of the digital number

Figure 5 illustrates a phase-locked loop including an incremental phase comparator, ie a phase comparator according to the invention As shown in the figure, the output of the incremental phase comparator (IPC) 501, i e is connected to a voltage controlled oscillator 503 via a loop filter 502 A reference signal is connected to a first input of the incremental phase comparator 501, i e to the input of the first register 208 (see figure 2, 3 or 4), and the output of the voltage controlled oscillator 503 is connected to a second input of the incremental phase comparator 501 via a frequency divider 504 As illustrated in figures 2, 3 and 4, the second input of the incremental phase comparator 501 may be connected to third register 211 Hereby, when an oscillation reference signal and an output signal of a voltage controlled oscillator is supplied as the first and the second input signals to the trigger means 205, 206, respectively, and when the second and the fourth registers 209, 212 are given a value representing a predefined phase step, the output of the first and the second accumulator represents an accumulated phase value of the reference signal and an accumulated phase value of the output of the voltage controlled oscillator, respectively

When comparing the phase-locked loop according to the invention with the prior art phase-locked loop of figure 1, it is found that the incremental phase comparator (IPC) replaces a phase detector according to the prior art, i e it has the same function as the prior art phase-locked loop of figure 1, but has a much better bandwidth and consequently faster lock-in time

The invention has been described with a preferred embodiment It is, however, possible to make changes and alterations to the shown example, while staying within the inventions idea As an example, it is in the above description hinted that the digital numbers in the registers always are the same or will only change occasionally It is, however, as an example possible to continuously change the digital numbers in the registers and thereby produce a pulse wide modulation of the output signal with the result that different phase and frequency modulation schemes (QPSK, FSK, GFSK,

etc) are achieved

Claims:

1 Phase-locked loop (100) comprising

a voltage controlled oscillator (101) for generating an output signal and having a frequency control input for controlling the frequency of the output signal,

a divider (102) for dividing the frequency of the output signal, and

a phase comparator (103) for deriving a control signal from a phase error detected between the frequency-divided output signal and a reference signal, said control signal being coupled to the frequency control input of said voltage controlled oscillator (101),

characterised in that the phase comparator (103) includes

a first accumulator (208) adapted to add a first predefined phase step value (209) to a first accumulated phase value in response to a reoccurring event in the reference signal,

a second accumulator (211) adapted to add a second predefined phase step value (212) to a second accumulated phase value in response to a reoccurring event in the frequency-divided output signal, and

subtracting means (223) for determining the phase error by subtracting the second accumulated phase value from the first accumulated phase value

2 Phase-locked loop (100) according to claim 1, characterised in that the phase comparator (103) includes a digital-to-analogue converter (204) adapted to convert the phase error and thereby to generate an analogue output signal

3 Phase-locked loop (100) according to claim 1, characterised in that the phase comparator (103) includes a first and a second digital-to-analogue converter (204A, 204B) adapted to convert the first and the second accumulated phase value and thereby to generate analogue representations thereof, and that the subtracting means (223) are adapted to perform an analogue subtraction of the analogue representation of the second accumulated phase value from the analogue representation of the first accumulated phase value

4 Phase-locked loop (100) according to claim 3, characterised in that the phase comparator (103) includes a first and a second AND-means (220, 221), where the output of said first AND-means (220) is connected to a first digital-to-analogue converter (204A), whereby a first accumulator (208) is connected to a first non-inverting input of said first AND-means (220) and whereby a second accumulator (211) is connected to a first inverting input of said first AND-means (220), the output of said second AND-means (221) being connected to said second digital-to-analogue converter (204B), and that said second accumulator (211) further is connected to a first non-inverting input of said second AND-means (221), said first accumulator (208) further being connected to a first inverting input of said second AND-means (221)

5 Phase-locked loop (100) according to claim 3 or 4, characterised in that the phase comparator (103) includes a first reset means for the most significant bit of the first accumulator, a second reset means for the most significant bit of the second accumulator, and a third AND-means (404), where the output of said third AND-means (404) is connected to said first and said second reset means of said first and said second accumulator (208, 211), where the most significant bit of said first accumulator (208) is connected to a first non-inverting input of said third AND-means (404), and where the most significant bit of said second accumulator (211) is connected to a second non-inverting input of said third AND-means (404)

6 A method for determining the phase error between a first signal and a second signal,

c h a r a c t e r i s e d in that it includes the steps of

frequency dividing the first signal and/or the second signal,

generating a first reoccurring trigger event in response to the first signal,

generating a second reoccurring trigger event in response to the second signal,

incrementing a first phase value by a first predetermined increment value when the first trigger event occurs,

incrementing a second phase value by a second predetermined increment value when the second trigger event occurs,

calculating said phase error by subtracting said second phase value from said first phase value

7 A method according to claim 6, c h a r a c t e r i s e d by representing the first phase value, the second phase value and the phase error by binary numbers

8 A method according to claim 7, c h a r a c t e r i s e d by calculating a first intermediary binary value as $I_1 = A_1 + \overline{A_2}$, by calculating a second intermediary binary value as $I_2 = \overline{A_1} + A_2$ and by calculating the phase error as $I_1 - I_2$

9 A method according to claim 7, c h a r a c t e r i s e d by resetting the most significant bit of the first phase value and the second phase value when the most significant bit of both said first phase value and said second phase value is simultaneously 1

10 A method according to claim 9, c h a r a c t e r i s e d in resetting two equal bits whenever these are 1 at the same time

11 Phase comparator (103) for carrying out the method in accordance to claim 6-10,

c h a r a c t e r i s e d in that the phase comparator (103) includes

a first accumulator (208) adapted to add a first predefined phase step value (209) to a first accumulated phase value in response to a reoccurring event in said reference signal,

a second accumulator (211) adapted to add a second predefined phase step value (212) to a second accumulated phase value in response to a reoccurring event in said input signal, and

subtracting means (223) for determining the phase error by subtracting the second accumulated phase value from the first accumulated phase value

12 Phase comparator (103) according to claim 11, c h a r a c t e r i s e d in that the phase comparator (103) includes a digital-to-analogue converter (204) adapted to convert the phase error and thereby to generate an analogue output signal

13 Phase comparator (103) according to claim 11, c h a r a c t e r i s e d in that the phase comparator includes a first and a second digital-to-analogue converter (204A, 204B) adapted to convert the first and the second accumulated phase value and thereby to generate analogue representations thereof, and that the subtracting means (223) are adapted to perform an analogue subtraction of the analogue representation of said second accumulated phase value from the analogue representation of said first accumulated phase value

14 Phase comparator (103) according to claim 13, c h a r a c t e r i s e d in that the phase comparator (103) includes a first and a second AND-means (220, 221), where the output of said first AND-means (220) is connected to a first digital-to-analogue converter (204A), whereby a first accumulator (208) is connected to a first non-inverting input of said first AND-means (220), and whereby a second accumulator (211) is connected to a first inverting input of said first AND-means (220), the output of said second AND-means (221) being connected to said second digital-to-analogue converter (204B), and that said second accumulator (211) further is connected to a first non-inverting input of said second AND-means (221), said first accumulator (208) further being connected to a first inverting input of said second AND-means (221)

15 Phase comparator (103) according to claim 13 or 14, c h a r a c t e r i s e d in that the phase comparator (103) includes a first reset means for the most significant bit of the first accumulator (208), a second reset means for the most significant bit of the second accumulator (211) and a third AND-means (404), where the output of said third AND-means (440) is connected to said first and said second reset means of said first and said second accumulator (208, 211), where the most significant bit of said first accumulator (208) is connected to a first non-inverting input of said third AND-means (404), and where the most significant bit of said second accumulator (211) is connected to a second non-inverting input of said third AND-means (404)

For Silicide A/S

Chas Hude A/S

ABSTRACT

The invention relates to a phase-locked loop comprising a voltage controlled oscillator and having a frequency control input for controlling the frequency of the output signal The phase-locked loop also has a frequency divider, and a phase comparator for deriving a control signal from a phase error detected between the frequency-divided output signal and a reference signal The control signal being coupled to the frequency control input of said voltage controlled oscillator The phase comparator includes a first and a second accumulator adapted to add a first or a second predefined phase step value to a first accumulated phase value The phase-locked loop has subtracting means for determining the phase error

The invention also relates to a method of for obtaining information on a phase error between two signals

The invention also relates to a phase comparator for use in a phase-locked loop

Figure 2 should be published

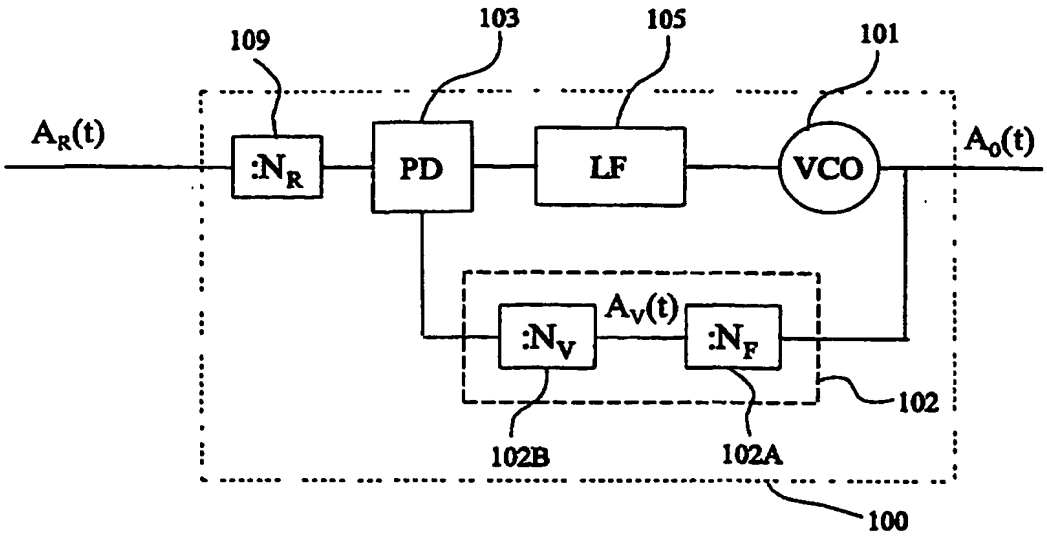

Fig. 1

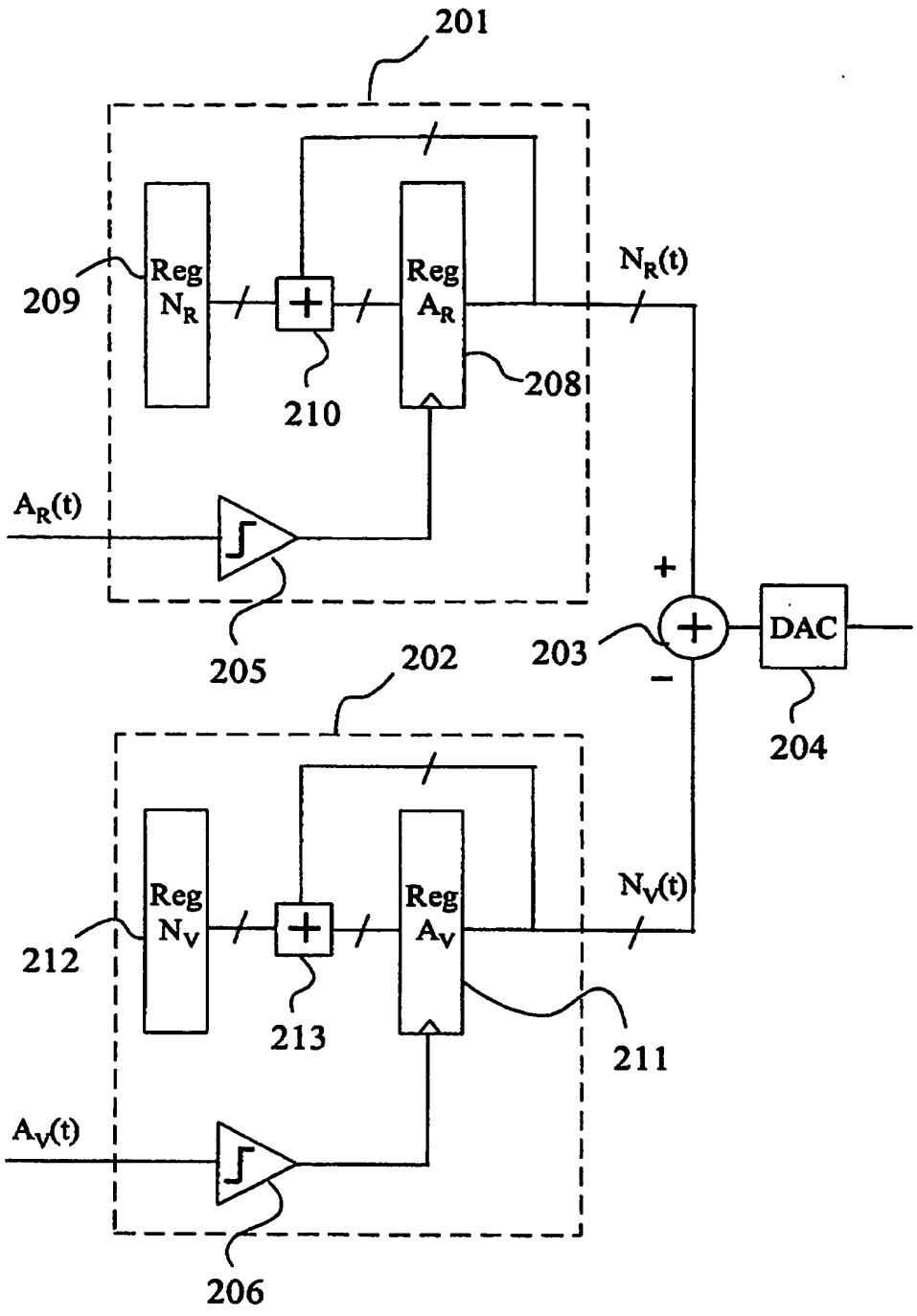

Fig. 2

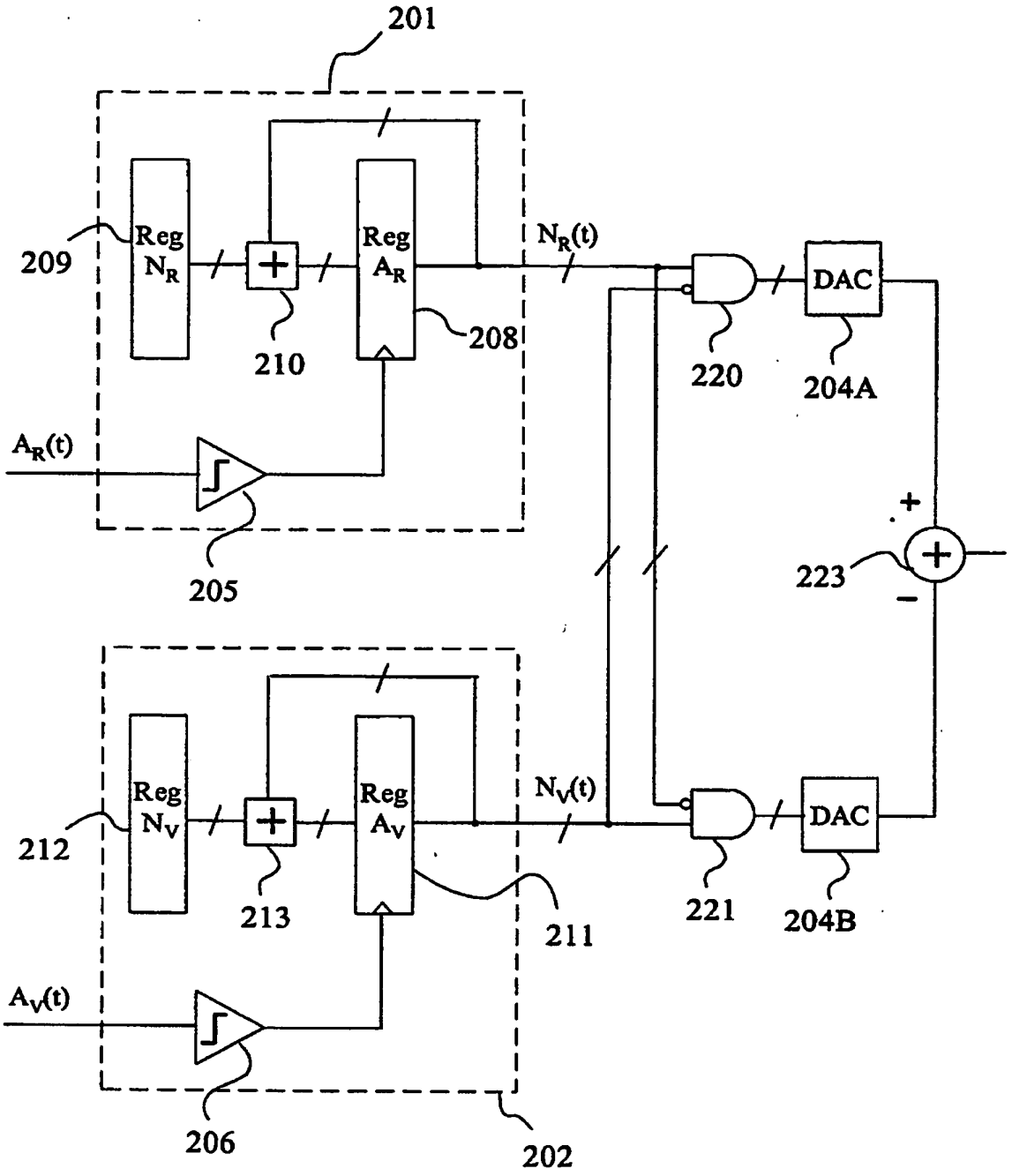

Fig. 3

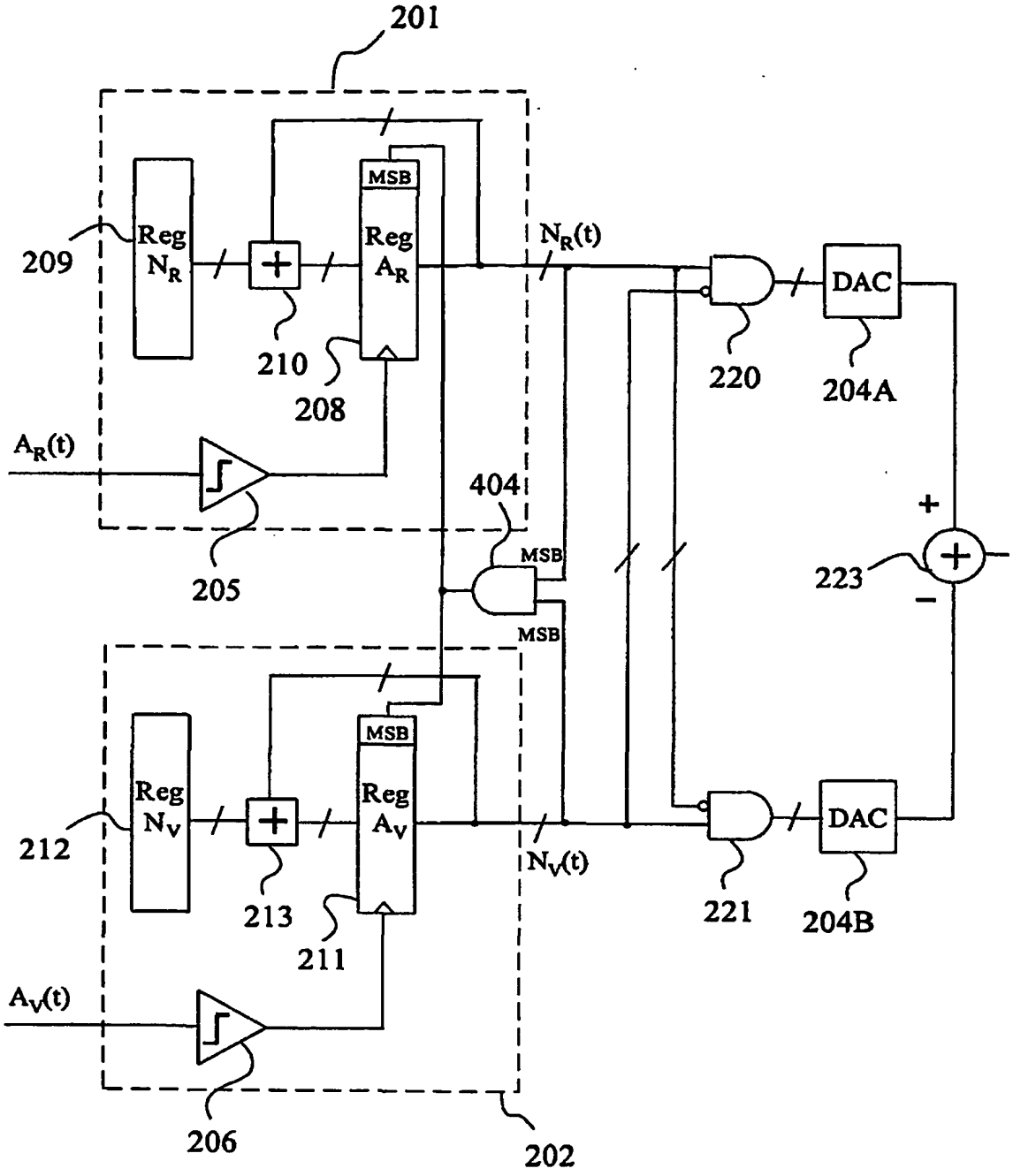

Fig. 4

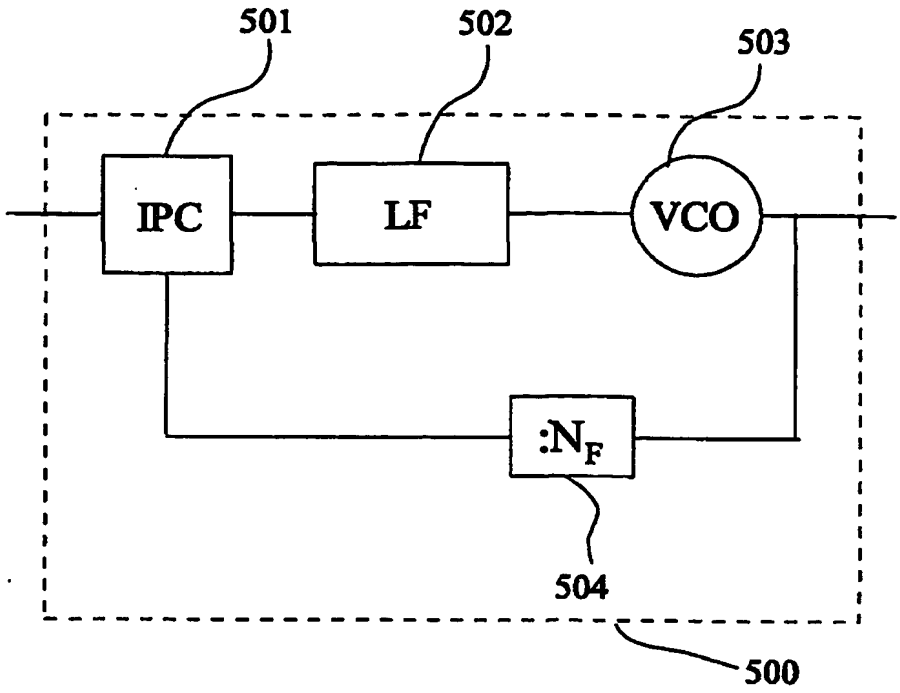

Fig. 5